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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

7590 08/25/2005

ON Semiconductor
Patent Administration Dept - MD A700
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Phoenix, AZ 85082-2890

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,145	AVERETT ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The indicated allowability of claims 1-9 and 26-32 is withdrawn in view of the newly discovered reference(s) to Davies (6,512,283) and Kadosh et al. (6,069,398). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 and 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davies (6,512,283) in view of Kadosh et al. (6,069,398).

Regarding claims 1 and 26, Davies teaches in figure 9 and related text a semiconductor device, comprising :

A semiconductor substrate 10 having a surface formed with a first recessed region 200;

a first dielectric material 15 deposited in the first recessed region and formed with a second recessed region 21 having walls;

a semiconductor layer formed in proximity to the second recessed region (column 4, lines 19-21); and

a thermal oxide layer 56 formed below the semiconductor layer, wherein the thermal oxide layer seals the second recessed region while leaving a void in the second recessed region.

Davies does not state that the thermal oxide layer is formed integral with the semiconductor layer (the resistor).

Kadosh et al. teach in figure 1C and related text a thermal oxide layer 26 is formed integral with a resistor 30 comprising a semiconductor layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the thermal oxide layer integral with the resistor in Davies's device in order to reduce the size of the device and in order to improve the characteristics of the device.

Regarding claims 2-8, 10, 27 and 29-33, Davies teaches an active device (figure 1) formed in an active region 11 of the semiconductor substrate, wherein an electrical component formed over the second recessed region, wherein the electrical component comprises a passive device or bonding pad of the semiconductor device, wherein the semiconductor layer comprises polysilicon, wherein the first dielectric material includes deposited silicon dioxide, and a layer of polysilicon material formed overlying the walls of the second recessed region, wherein the first dielectric material is recessed below a major surface of the semiconductor substrate.

Regarding claim 9, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recess the first dielectric material below the major surface a distance of about 0.5 microns in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

Regarding claim 28, the process limitations of "thermally grown silicon dioxide" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Claims 1-10 and 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. (5,640,041).

Lur et al. teach in figure 14 and related text a semiconductor device, comprising:

A semiconductor substrate 1 having a surface formed with a first recessed region 16;

a first dielectric material deposited in the first recessed region and formed with a second recessed region 19 having walls;

a semiconductor layer 5 formed in proximity to the second recessed region; and a thermal oxide layer 25 formed integral with the semiconductor layer, wherein the thermal oxide layer seals the second recessed region while leaving a void 8 in the second recessed region.

Lur et al. do not state that the thermal oxide layer is formed integral with the semiconductor layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the thermal oxide layer integral with the semiconductor layer in Lur et al.'s device in order to improve the characteristics and the integrity of the device.

Regarding claims 2-8, 10, 27 and 29-33, Lu et al. teach an active device 5 formed in an active region of the semiconductor substrate, wherein an electrical component 5 formed over the second recessed region, wherein the electrical component comprises a passive device 56 or bonding pad of the semiconductor device, wherein the semiconductor layer comprises polysilicon, wherein the first dielectric material includes deposited silicon dioxide, and a layer of polysilicon material formed overlying the walls of the second recessed region, wherein the first dielectric material is recessed below a

major surface of the semiconductor substrate.

Regarding claim 9, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recess the first dielectric material below the major surface a distance of about 0.5 microns in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

Regarding claim 28, the process limitations of "thermally grown silicon dioxide" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-E are cited as being related to STI comprising voids.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
8/23/05

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